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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
FIS920040005US1

In Re Application Of: Jochen Beintner, et al.

FEB 02 2005

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/709,963	June 9, 2004	Unassigned	23389	2812	3962

Title: RAISED STI PROCESS FOR MULTIPLE GATE OX AND SIDEWALL PROTECTION ON STRAINED Si/SiGOI STRUCTURE WITH ELEVATED SOURCE/DRAIN

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Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

- the statement specified in 37 CFR 1.97(e);

OR

- the fee set forth in 37 CFR 1.17(p).

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

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Signature of Person Mailing Correspondence

Leslie S. Szivos, Ph.D. Reg. No. 39,394

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Dated: January 27, 2005

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Applicants:

Jochen Beintner, et al.

Examiner: Unassigned

Serial No:

10/709,963

Art Unit: 2812

Filed:

June 9, 2004

Docket: FIS920040005US1 (17369)

Dated:

January 27, 2005

For:

RAISED STI PROCESS FOR MULTIPLE GATE OX AND SIDEWALL PROTECTION ON STRAINED Si/SGOI STRUCTURE WITH ELEVATED SOURCE/DRAIN

INFORMATION DISCLOSURE STATEMENT

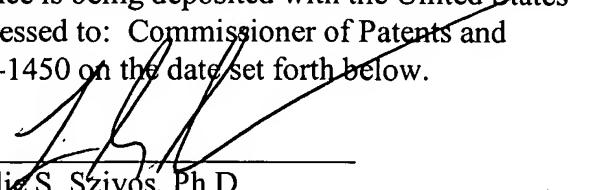
Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, applicants submit the following references which applicants believe may be material to the above-identified patent application. A copy of the references which applicants wish to make of record in this case is enclosed herein for the Examiner's convenience along with a listing on Form PTO-1449 attached.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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Dated: January 27, 2005


Leslie S. Szivos, Ph.D.

1. U.S. Patent No. 3,602,841, dated August 31, 1971, issued to McGroddy;
2. U.S. Patent No. 4,665,415, dated May 12, 1987, issued to Esaki, et al.;
3. U.S. Patent No. 4,853,076, dated August 1, 1989, issued to Tsaur, et al.;
4. U.S. Patent No. 4,855,245, dated August 8, 1989, issued to Neppl, et al.;
5. U.S. Patent No. 4,952,524, dated August 28, 1990, issued to Lee, et al.;
6. U.S. Patent No. 4,958,213, dated September 18, 1990, issued to Eklund, et al.;
7. U.S. Patent No. 5,006,913, dated April 9, 1991, issued to Sugahara, et al.;
8. U.S. Patent No. 5,060,030, dated October 22, 1991, issued to Hoke;
9. U.S. Patent No. 5,081,513, dated January 14, 1992, issued to Jackson, et al.;
10. U.S. Patent No. 5,108,843, dated April 28, 1992, issued to Ohtaka, et al.;
11. U.S. Patent No. 5,134,085, dated July 28, 1992, issued to Gilgen, et al.;
12. U.S. Patent No. 5,310,446, dated May 10, 1994, issued to Konishi, et al.;
13. U.S. Patent No. 5,354,695, dated October 11, 1994, issued to Leedy;
14. U.S. Patent No. 5,371,399, dated December 6, 1994, issued to Burroughes, et al.;
15. U.S. Patent No. 5,391,510, dated February 21, 1995, issued to Hsu, et al.;
16. U.S. Patent No. 5,459,346, dated October 17, 1995, issued to Asakawa, et al.;

17. U.S. Patent No. 5,471,948, dated December 5, 1995, issued to Burroughes, et al.;
18. U.S. Patent No. 5,557,122, dated September 17, 1996, issued to Shrivastava, et al.;
19. U.S. Patent No. 5,561,302, dated October 1, 1996, issued to Candelaria;
20. U.S. Patent No. 5,565,697, dated October 15, 1996, issued to Asakawa, et al.;
21. U.S. Patent No. 5,571,741, dated November 5, 1996, issued to Leedy, et al.;
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24. U.S. Patent No. 5,670,798, dated September 23, 1997, issued to Schetzina;
25. U.S. Patent No. 5,679,965, dated October 21, 1997, issued to Schetzina;
26. U.S. Patent No. 5,683,934, dated November 4, 1997, issued to Candelaria;
27. U.S. Patent No. 5,840,593, dated November 24, 1998, issued to Leedy;
28. U.S. Patent No. 5,861,651, dated January 19, 1999, issued to Brasen, et al.;
29. U.S. Patent No. 5,880,040, dated March 9, 1999, issued to Sun, et al.;
30. U.S. Patent No. 5,940,736, dated August 17, 1999, issued to Brady, et al.;
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33. U.S. Patent No. 5,989,978, dated November 23, 1999, issued to Peidous;

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40. U.S. Patent No. 6,117,722, dated September 12, 2000, issued to Wuu, et al.;
41. U.S. Patent No. 6,133,071, dated October 17, 2000, issued to Nagai;
42. U.S. Patent No. 6,165,383, dated December 26, 2000, issued to Chou;
43. U.S. Patent No. 6,221,735, dated April 24, 2001, issued to Manley, et al.;
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54. U.S. Patent No. 6,361,885, dated March 26, 2002, issued to Chou;
55. U.S. Patent No. 6,362,082, dated March 26, 2002, issued to Doyle, et al.;
56. U.S. Patent No. 6,368,931, dated April 9, 2002, issued to Kuhn, et al.;
57. U.S. Patent No. 6,403,486, dated June 11, 2002, issued to Lou;
58. U.S. Patent No. 6,403,975, dated June 11, 2002, issued to Brunner, et al.;
59. U.S. Patent No. 6,406,973, dated June 18, 2002, issued to Lee;
60. U.S. Patent No. 6,461,936, dated October 18, 2002, issued to Von Ehrenwall;
61. U.S. Patent No. 6,476,462, dated November 5, 2002, issued to Shimizu, et al.;
62. U.S. Patent No. 6,493,497, dated December 10, 2002, issued to Ramdani, et al.;
63. U.S. Patent No. 6,498,358, dated December 24, 2002, issued to Lach, et al.;
64. U.S. Patent No. 6,501,121, dated December 31, 2002, issued to Yu, et al.;
65. U.S. Patent No. 6,506,652, dated January 14, 2003, issued to Jan, et al.;
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68. U.S. Patent No. 6,531,369, dated March 11, 2003, issued to Ozkan, et al.;
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73. U.S. Patent Application Publication No. 2002/0086497 A1, dated July 4, 2002, issued to Kwok;
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78. U.S. Patent Application Publication No. 2003/0067035 A1, dated April 10, 2003, issued to Tews, et al.; and
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80. Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si *n*-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998;

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82. Scott, et al. "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999;
83. Ootsuka, et al. "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Device Meeting, 23.5.1, IEEE, April 2000;
84. Ito, et al. "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000;
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87. Ouyang, et al. "Two-Dimensional Bandgap Engineering in a Novel Si/SiGe pMOSFETS With Enhanced Device Performance and Scalability", Microelectronics Research Center, pp 151-154, 2000 IEEE.
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89. European Patent Application Publication No. EPO 01/62362, 26/06/89, issued to Hasegawa, Michihiko;
90. European Patent Application Publication No. EP 1 174 928 A1, dated 01/23/02, issued to Hitachi Ltd.;
91. European Patent Application Publication No. EP 0 967 636 A2, dated 12/29/1999, issued to Rengarajan, et al.;

92. International Patent Application Publication No. WO 02/454156 A2, dated 06/06/2002, issued to Armstrong et al.;
93. International Application Publication No. WO 94/27317, dated 05/06/1993, issued to Winnerl, et al.;

Applicant is submitting copies of the above-cited non-U.S. Patent references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

In accordance with the waiver of 37 C.F.R. § 1.98 (a)(2)(i), per 1276 OG 55, August 5, 2003, applicants are not required to submit copies of the above-cited U.S. Patent references.

Respectfully submitted,

Leslie S. Szivos
Registration No. 39,394

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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. FIS920040005US1 (17369)	SERIAL NO. 10/709,963
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANTS Jochen Beintner, et al.	
(Use several sheets if necessary)		FILING DATE June 9, 2004	GROUP ART UNIT 2812

U.S. PATENT DOCUMENTS

EXAMINEE INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,602,841	08/31/71	McGroddy			
	4,665,415	05/12/87	Esaki, et al			
	4,853,076	08/01/89	Tsaur, et al			
	4,855,245	08/08/89	Neppl, et al			
	4,952,524	08/28/90	Lee, et al			
	4,958,213	09/18/90	Eklund, et al			
	5,006,913	04/09/91	Sugahara, et al			
	5,060,030	10/22/91	Hoke			
	5,081,513	01/14/92	Jackson, et al			
	5,108,843	04/28/92	Ohtaka, et al			
	5,134,085	07/28/92	Gilgen, et al			
	5,310,446	05/10/94	Konishi, et al			
	5,354,695	10/11/94	Leedy			
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	5,679,965	10/21/97	Schetzina			
	5,683,934	11/04/97	Candelaria			
	5,840,593	11/24/98	Leedy			
	5,861,651	01/19/99	Brasen, et al			
	5,880,040	03/09/99	Sun, et al			

Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with NPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use several sheets if necessary)

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	5,989,978	11/23/99	Peidous				
	6,008,126	12/28/99	Leedy				
	6,025,280	02/15/00	Brady, et al				
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	6,255,169	07/03/01	Li, et al				
	6,261,964	07/17/01	Wu, et al				
	6,265,317	07/24/01	Chiu, et al				
	6,274,444	08/14/01	Wang				
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	6,284,623	09/04/01	Zhang, et al				
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	6,319,794	11/20/01	Akatsu, et al				
	6,361,885	03/26/02	Chou				
	6,362,082	03/26/02	Doyle, et al				
	6,368,931	04/09/02	Kuhn, et al				
	6,403,486	06/11/02	Lou				
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	6,406,973	06/18/02	Lee				
	6,461,936	10/18/02	Von Ehrenwall				
	6,476,462	11/05/02	Shimizu, et al				

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	6,493,497	12/10/02	Ramdani, et al			
	6,498,358	12/24/02	Lach, et al			
	6,501,121	12/31/02	Yu, et al			
	6,506,652	01/14/03	Jan, et al			
	6,509,618	01/21/03	Jan, et al			
	6,521,964	02/18/03	Jan, et al			
	6,531,369	03/11/03	Ozkan, et al			
	6,531,740	03/11/03	Bosco, et al			
U.S. PATENT APPLICATION PUBLICATION DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	2001/000978 4 A1	07/26/01	Ma, et al			
	2002/007459 8 A1	07/20/02	Doyle, et al			
	2002/008647 2 A1	07/04/02	Roberds, et al			
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	2003/006703 5 A1	04/10/03	Tews, et al			
Examiner			Date Considered			
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(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEAtty. Docket No.
FIS920040005US1 (17369)Serial No.
10/709,963LIST OF PRIOR ART
CITED BY APPLICANT

(Use several sheets if necessary)

Applicants
Jochen Beintner, et al.Filing Date
June 9, 2004Group
2812

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		EPO 01/62362	26/06/89	Europe				
		EP 1 174 928 A1	01/23/02	Europe				
		EP 0 967 636 A2	12/29/1999	Europe				
		WO 02/454156 A2	06/06/2002	PCT				
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	Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998
	Rim, et al. "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99
	Scott, et al. "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999
	Ootsuka, et al. "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Device Meeting, 23.5.1, IEEE, April 2000
	Ito, et al. "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000
	Shimizu, et al. "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001
	Ota, et al. "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002
	Ouyang, et al. "Two-Dimensional Bandgap Engineering in a Novel Si/SiGe pMOSFETs With Enhanced Device Performance and Scalability", Microelectronics Research Center, pp 151-154, 2000 IEEE
	Sayama et al., "Effect of <Channel Direction for High Performance SCE Immune pMOSFET with Less Than 0.15um Gate Length" ULSI Development Center, pp27.5.1-27.5.4, 1999 IEEE

EXAMINER

DATE CONSIDERED

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